FORM PTO-1449 (REV. 7-80)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.	APPLICATION NO.
51889/3 US	10/719,119

APPLICANT – Douglas R. Hackler, Sr. et al.

FILING DATE- November 21, 2003

INFORMATION DISCLOSURE CITATION

Title: **DOUBLE-GATED TRANSISTOR CIRCUIT**

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
PV	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
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PC	90	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1μm Regime," Microelectronics Engineering Laboratory, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.3.1-29.3.4.
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PC	A15	4,468,574	08/28/84	Engeler et al.	307	451	05/03/82
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